UNITED STATES PATENT APPLICATION

of

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for a

LOW VOLTAGE DIFFERENTIAL IN DIFFERENTIAL OUT RECEIVER

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RELATED APPLICATIONS

The present application is a continuation in part (CIP) of U.S. patent application serial no. 10/282,569 filed Oct. 29, 2003, entitled "Low Power Low Voltage Differential Signal Receiver with Improved Skew and Jitter Performance." This application is commonly owned and shares an inventor with the present application. The present application is also related to U.S. patent application, entitled Low Power, Low Voltage Differential Receiver, co-filed with the present application and of common inventorship and ownership.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to interface circuits, and more particularly to Input/Output (I/O) circuits and receivers, and even more particularly to high speed, low voltage, low power, differential input, low jitter and skew I/O receiver circuits that provide a differential output (LVDO).

Background Information

Low voltage differential signals are common for high-speed signal transmission. Saturation effects are avoided and power dissipation is limited, and, since low voltage signals are prone to noise, use of differential signals, where the noise is common to both signals, generally overcomes this problem.

However, since common mode signals will occur, LVDO circuits are designed to accept differential signals that ride on a common mode level that may range from the low power (ground) rail to the Vcc power rail.

U.S. Patent Nos. 5,801,564; 6,252,432 B1 and 6,236,269 B1 set out a high speed circuits that operate over a wide input common mode range where each has a differential input and a single ended output. In these patents the differential input signals connect to gates of both an NMOS and a PMOS transistor pair connected source to source, where the NMOS pair handle common mode voltages up to within about 200 millivolts of the high power rail and the PMOS pair down to within about 200 millivolts of the ground. A second stage converts the differential input to a rail to rail single output signal suitable for driving CMOS inverters. This large output signal dynamic range requires a high gain second stage that reduces the frequency response. Moreover, the combined effect of input signal common mode level on the second stage, and second stage wide dynamic output range, limits practical circuits to higher Vcc levels. Also, when the common mode input voltage and the second stage output voltage change from the ground rail to the Vcc rail, the cross over (switching point) point for the circuit changes since the currents, the gain, and the impedances all change. This crossover point change increases jitter. If the currents were unchanged over the range of input signal common mode voltage swing, the gains would be about constant thereby reducing jitter over that range of input common mode levels.

There is a need for a differential low voltage receiver with a wide input signal common mode range with a differential output and that reduces power dissipation, skew and jitter, and that operates at lower Vcc levels but maintains high speed (high frequency) operation.

It will be appreciated by those skilled in the art that although the following Detailed Description will proceed with reference being made to illustrative embodiments, the drawings, and methods of use, the present invention is not intended to be limited to these embodiments and methods of use. Rather, the present invention is of broad scope and is intended to be defined as only set forth in the accompanying claims.

SUMMARY OF THE INVENTION

In view of the foregoing background discussion, the present invention provides a high speed, low voltage, low power, differential receiver that provides lower skew and jitter over a wide range of common mode input signal levels. The present invention also provides a lower output voltage swing from the second stage that improves the low Vcc performance of the invention.

The present invention includes a folded cascode made up of a differential input stage and a load or current summation stage, and a second differential stage. The differential input stage includes first NMOS pair and a PMOS pair of differentially connected transistors that accept a rail to rail input common mode signal level. The load or summation stage follows with a full ground to Vcc output signal only at thesecond differential stage . This arrangement provides a lower gain second stage with a lower output voltage swing, lower power dissipation, better crossover control, high speed, and better jitter and skew performance.

The differential input and load or current summation stages share current sources, and the differential signal is transferred between these stages via these shared current sources. The better performance is due partly to keeping the current sources substantially constant over a wider range of common mode input voltage levels. The reduced signal voltage swings of the load or summation stage allows the current sources to remain operational over a wider range of input common signal levels and at lower Vcc levels than if the output of that stage traversed from ground to Vcc. The reduced load or summation stage output voltage swing also benefits by keeping impedances and cross over points relatively constant over wider ranges of common mode signal levels. The second differential stage does not share currents and is relatively unaffected by the input common mode signal level. This stage provides a differential output signal with higher voltage drive for complementary CMOS inverters that provide a differential output signal, but with the higher currents available this stage performs at high frequencies and its input

differential switching threshold remains substantially constant and does not appreciably affect the crossover point.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention description below refers to the accompanying drawings, of which:

FIG. 1 is a circuit block diagram of the present invention;

FIGS. 2A and 2B are schematic of the parallel paths in the load or current stage of a preferred embodiment; and

FIG. 3A, 3B, and 3C are several preferred second differential stages.

FIG. 4 is a chart of skew performance over Vcc; and

FIG. 5. more detailed circuit schematic of the circuit of FIG. 1.

DETAILED DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

FIG. 1 is a schematic block diagram of a folded cascode 2 comprised of source coupled NMOS transistors, N1 and N2, with a current source I2 connecting the sources to ground. There is a parallel set of PMOS transistors, P1 and P2, sharing a current source I1 connecting their sources to the power rail, Vcc. I1 and I2 are complementary current sources, typically of equal value. The value may range widely from microamps to milliamps or more depending on applications. In one preferred embodiment I1 and I2 are arranged to provide 0.350 milliamps. The gates of N1 and P1 are connected together and to an input signal, In+, and the gates of N2 and P2 are similarly connected together and to the complementary input signal, In-. Each of the drains of the input stage NMOS and PMOS transistors are connected together, in a folded cascode fashion, to sources of opposite polarity transistors in the load or current summation stage 4. Folded cascode circuits have the beneficial characteristic of a differential input voltage signal input to high impedance gates (or bases, in bipolar circuits) causing an output differential current from their high impedance drains that is fed into low impedance sources. If there were a resistance or other such high impedance loads on the drains, an inverted voltage signal

would appear at the drains magnifying the Miller capacitance and thereby limiting the circuit's frequency range. Since the load on the drains are low impedance sources little or no voltage signal appears at the drains of the NMOSs and the Miller capacitance is nullified.

"Designs of Analog CMOS Integrated Circuits" by Behzad Razavi published by McGraw-Hill is a good reference describing folded cascode circuitry and is hereby incorporated herein by reference.

A preferred embodiment of the present invention, as in FIG. 1, has the input NMOS, N1, drain connected to the sources of PMOSs, SP2 and SP4. The drain of NMOS, N2, is similarly connected to the sources of PMOSs, SP1 and SP2. Also, from the input PMOS, P1, drain is connected to the sources of NMOS, SN2 and SN4, and the drain of PMOS, P2, is similarly connected to the sources of NMOS, SN1 and SN2.

In a preferred embodiment, the signal paths are equally balanced between the NMOS and the PMOS circuitry. I1 and I2 are set equal, and I3, I4, I5 and I6 are four complementary current sources that are usually set equal to each other and typically at higher value compared to I1 and I2. In one preferred embodiment each is 0.420 micro-amps. Other ratios may be used for other preferred embodiments. At quiescence balance I2 is drawn equally from I3 and I4, and I1 flows equally to I5 and I6. The remaining portion of I3 supplies I5 and that of I4 supplies I6. As practitioners in the art will understand, the current sources are MOS devices configured shown in FIG. 8. Also, as well known in the art, these current sources are operational over a range of voltages, but at some voltages they begin to demonstrate a resistive component.

The input NMOS pair of FIG. 1 allows the common mode input voltage to run at least to Vcc, and the PMOS pair of FIG. 1 allows the common mode input voltage to run at least to ground with acceptable circuit operation. The input NMOS transistors are identical with each other, as are the input PMOS transistors to make the circuits as symmetrical as possible. This parallel combination of differential input circuits allows the input common mode voltage to traverse at least from ground to Vcc. This can be seen from FIG. 1 where, if In+ and In- were both at Vcc, the current source I3 would still op-

erate supplying currents to I2 and to SP2 and SP4. Similarly, I4 will supply current to I2 and to SP1 and SP3. As is evident from the schematic, if there were a differential input voltage the currents from I3 and I4 would unequally supply currents for I2 and the remaining currents to SP1, 2, 3 and 4 in proportion to the differential input signal value.

Similarly, if the input In+ and In- were both at about ground, I5 and I6 would still operate in conjunction with SN1, 2, 3, and 4. With a differential between In+ and In-, I5 and I6 would unequally supply currents to I1, with the remaining portions to SN1, 2, 3, and 4.

FIGS. 2A and 2B show the load or current summation stage "unwrapped." With respect to FIG. 2A, SP4 and SN4 form a parallel current path with SP2 and SN2, where the current in SP4 is proportionally smaller but mirrored in SP2 and the current in SN4 is proportionally smaller but mirrored in SN2. The mirrored current values are proportional but are usually made unequal by the sizes of the transistors involved. As is evident from the circuit of FIG. 2 the current through these parallel paths is I3 minus Ia, where Ia is a portion of I2 as determined from the state of thefolded cascode stage 2. The current through these parallel paths is also equal to I5 plus Ib, where Ib is a portion of I1 as determined by the state of the cascode stage. So (I3 minus Ia) will equal (I5 plus Ib) until the input voltage levels interfere with the current sources. From a quiescent point, if Ia increases due to In+ increasing (N1 on harder) with respect to In-, then correspondingly Ib will decrease also due to In+ increasing (P1 on less hard). With I10 and I12 reduced at the top of the circuit FIG. 2A, but I5 drawing more current from I10 and I12 at the bottom of the circuit, om will fall in level. Obviously I5 will pull down om to a level where the voltage at I5 causes I5 to lower its nominal value due to a resistive component. The net effect is that I10 and I12 match the currents I3 minus I2 and I5 minus Ib. Similarly, I14 and I16 increases since Ia' is reduced (N2 on less hard) and Ib' increases (P2 on harder) and op will rise. In this instance I4 will demonstrate a resistive component.

With respect to FIGS. 1, 2A and 2B, the physical sizes of the transistors involved acting as current mirrors, as is known in the art, will determine the split in current between the two legs. For example I12 may be ten percent and I10 ninety percent of (I3-

Ia). Virtually any split may be accomplished by sizing the transistors involved. Also, by setting the current through SP2 and SN2 the resulting voltage at om is determined. Similarly the voltage at op is determined by the current through SP3 and SN3. The actual current levels of the current sources I1- I6, and the ratio of currents between the two parallel paths may be designed for virtually any levels consistent with the processes and circuit operation specifications desired. Higher currents will tend to increase gain/bandwidth but at high power dissipation. Higher current ratios of I10 to I12 and of I14 to I16 – current in the parallel paths, will tend to increase gain at the expense of bandwidth

In FIG. 2A and 2B, notice that the gates 20 and 30 are tied together via the connection 10. This has the desirable effect of allowing better control of the differential gains in the two circuits and better symmetry.

The voltage gain from In+ and In- to op and om is determined by the currents involved and the sizing of the transistors involved. In other circuits, as mentioned above, op and om may have driving CMOS gates and would be designed to swing from rail to rail. But, in an example of the present invention, a second differential stage is employed, item 6 in FIG. 1. Use of this second stage allows the voltage swing at op and om to be much reduced allowing lower currents, voltage levels and voltage swings to be designed. This improves bandwidth (since less gain), lowers power dissipation (less current), reduces skew and jitter (since the crossover point is better defined), and with the reduced voltage levels and swing the circuit will operate at a lower Vcc.

The overall circuit symmetry also provides low skew and low jitter performance. Here "symmetrical" refers to the parallel circuitry of the In+ or the In- signal paths being identical mirrors of each other including signal path lengths. That is, N1 is an identical mirror of N2, P1 of P2, SP1 of SP4. SN1 of SN4, SP2 of SP3, SN2 of SN3, and so on throughout the biasing and signal path lengths. In the present invention the differential output from the load or current summation stage, op/om, is input to a second differential stage 6, see FIG. 1. Several examples of a preferred second differential stage are shown in FIGS. 3A, 3B, and 3C, see below.

With reference to FIGS. 2A and 2B, the right hand sides carrying I12 and I16 are identically laid out as are the left-hand sides carrying I10 and I14. Moreover, the circuit of FIG. 2A is identically arranged as the circuit of FIG. 2B. In one preferred embodiment, the current sources (I1-I6) are 0.350 milliamps each, but other sizes, current ranges and at other proportions may be used to advantage in the present invention.

In this application SP1 and SN1 form a biasing current mirror leg for the signal path SP3 and SN3, as do SP4 and SN4 for the signal path SP2 and SN2.

Expanding on the symmetry discussion, in FIG. 1, following the circuitry from the input through to the output the circuitry is identical and symmetrical so that the loading on each transistor in the two differential paths. Moreover, the layout signal path lengths are designed to be virtually identical. This means that the transistor sizes and parameters, the capacitances, resistances and layout path lengths are all identical along both the In+ and the In- signal paths. This designed symmetry leads to minimized skew.

Jitter is an apparent signal riding on an actual differential signal causing variations in its period. One factor causing jitter is noise. One common source of noise is the power rail, Vcc. The circuit topology and component parameters are made symmetrical so that any signal riding on the power rail appears equally on both sides of the circuitry or in common mode and therefore its contribute to the differential signal is minimized. This factor is called the "power supply rejection ratio," which is the signal gain (output signal value divided by the input signal value divided by a valued calculated from an output signal value due to a signal on the power rail - basically the gain from the power rail to the output).

FIG. 3A shows a differential second stage that accepts the om signal at the gates of two PMOS transistors, P11 and P13, while the op signal is input to two other PMOS transistors, P10 and P12. A diode connected NMOS, N10, accepts the drain current from P10 and the current mirror N11 accepts the drain current from P11. N13 is another diode connected NMOS accepting the drain current from P13 while its current mirror N12 accepts the drain current from P12. In operation the current source I7 provides current regardless of the state of op and om, and so power is constantly being expended. In opera-

tion if om is low turning on P11 and P13, and op is high turning off P10 and P12, I7 current will run through P11 and P13. P13 drain current runs through N13 and turns on N12 which drive dm low. P11 current tries to run through N11, but N11 is off since N10 has no drain current, P10 being off. In this case P11 drain current charges up the capacitance at the node at the drains of P11 and N11, thus driving dp high. In this state all I7 travels through P13 and N13. Similar operation occurs when op is low and om high.

FIG. 3C is another preferred embodiment that is more power efficient than FIG. 3A. Here operation is identical with FIG. 3A, except two additional PMOS switches P20 and P21 are added. When om is low, dm goes low turning on P20 and dp goes high turning off P21 breaking that existed in FIG. 3A the current path for I7. In such a case I7 becomes starved and acts as a resistor, but only transient current exists thereby reducing the power dissipation.

Fig. 3B is another alternative to reduce the power consumption of FIG. 3A. Here, when om is low, I7 travels through P14 driving dp positive. N16 is turned on driving dm low turning off N15 thereby breaking the current path to ground. N14 is a diode connected NMOS and will maintain a current path through P14 to support I7. However, N14 may be designed to not accommodate I7 in full. In such a case I7 becomes a resistive but will maintain dp high. P15 is off since op is high. P15, N15 and N17 perform corresponding functions when op go low. The diode connected transistors N14 and N17 maintain and current path for I7 in the two cases. This circuit arrangement provides for higher switching speeds at the expense of some DC power dissipation.

As explained before, for FIG. 3A, the current split between the on PMOS transistors on side of the circuit will accept the current I7. The actual voltage level will be dependent on the sizes and construction of the PMOS and NMOS transistors in that leg, as is known in the art. A differential output is taken from the drains of P11 and P12, and, via the inverters shown in FIG. 1, lead to the differential outputs OUT + and OUT -. The circuit of FIG. 3A, as can be seen from the current source I7, that always drives current from Vcc to ground, this circuit consumes more power, compared to FIG. 3B and 3C.

FIG. 4 represents skew performance improvement where the trace 34 indicates lower skew as compared to prior art designs 32. Notice that FIG. 4 has data points at Vcc of 1.4 volts where the prior art designs will not operate. This is due in part to the reduced swings at op and om, where a differential swing of 0.250 between op and om suffices to guaranty switching of the second differential stage.

The differential voltage gain of the folded cascade stage from (In+ minus In-) to (op minus om) is determined by the transconductance of the differential input stage and by the effective transresistance of the load or current summation stage– the value of op and om as determined by the currents through the parallel paths of FIG. 2A and FIG. 2B. Still referring to FIG. 2A the current through each leg I10 and I12 is a function of the current sources and the sizes of the transistors, as is known in the art. In this fashion the voltage gain can be trimmed to a value that preserves high speed operation, wide input common mode levels, and lower power supply operation, together with better skew and jitter performance. In a preferred embodiment, the current sources and the sizes can be selected so that the input common mode level can run from ground to Vcc and the common mode level of op and om remains well within a few hundred millivolts. This allows the circuit to operate with a Vcc e as low as +1.4V. Moreover, the differential output of the load or current summation stage 4 can be set so that the maximum differential output (op minus om) can be set to a few hundred millivolts. Of course other values can be used in other preferred embodiments. FIG. 1 shows an output differential stage 6 with inputs of op and om and outputs dp and dm and, via inverter chains, out+ and out-. Moreover, the common mode gain, the common mode input to the common mode output of the load or current summation stage can be kept well above ground and well below Vcc, as is known in the art, so that the circuit operates at a lower Vcc than prior art circuits.

From FIG. 1, the gates of all the transistors in the load or current summation stage are connected together. Also, the outer transistors, SP1, SP4, SN1, and SN4 are the biasing legs with their drains and their gates all interconnected with each other. These outer transistors bias the inner transistors, SP2, SP3, SN2, and SN3 that carry a proportional mirrored current, and with the currents differentially distributed, dependent on the input differential signal. The biasing transistors determine the signal at the drains of the

inner transistors. This common gate/drain connection allows better control for better symmetry of the differential outputs op and om, thereby improving skew and jitter.

FIG. 5 is a more detailed schematic of FIG.1, although the second of the two series inverters is not shown. Here the same biasing and signal MOS transistors are shown as described with respect to FIGS. 1, 2A and 2B. The current source I1- I7 are shown as PMOS and NMOS transistors. The PMOS M3 and NMOS M4 configured between ground and Vcc provide the reference biasing for the current sources as is known in the art.

Back to FIG. 1, it is helpful review the circuit operation and follow a signal through the schematic. Here a differential signal at a common mode voltage of Vc/2 will be described traveling through the NMOS transistors, N1 and N2. There will be a corresponding equivalent signal path through P1 and P2.

For description purposes consider both inputs at Vcc/2 and both outputs op and om at Vcc/2 also. This state will typically only exist transiently during switching but the distribution of currents will be clear from the circuitry and from there the differential signals will be evident. In this preferred embodiment example, consider I1 and I2 to be 0.35 milliamps, and I3, I4, I5, and I6 to be 0.420 milliamps. In this balance condition, one half of I2 is supplied equally from I3 and I4 through N1 and N2. And one half of I1 is supplied equally to I5 and I6 through P1 and P2. The remaining portions of I3 supplies the remaining portion of I5, and the remaining portion of I4 supplies the remaining portion of I6, as can be seen from FIGS. 2A and 2B.

Now, from FIGS. 1, 2A and 2B, if In+ is slightly higher than In-, more of I3 travels through N1 leaving less for I10 and I12, and more of I4 will travel through I14 and I16 and less through N2. Similarly, if In+ is higher than In-, more of I6 travels through P2 leaving less for I14 and I16, and more of I5 will travel through I10 and I12. The result is a higher op with respect to om.

With a large enough differential all of I2 travels through N1 and is supplied from I3 leaving a remainder current for I10 and I12, and correspondingly all on I4 travels through I14 and I16. In this case, with matched current source, all of I1 runs through P2

to I6 and I14 and I16 are reduced and om is lowered. All of I5 travels through I10 and I12 and op is raised. It is evident from such a condition that if I5 is equal to I3 and less of I3 flows into the load or current summation stage paths and more of I5 flow flows from the same paths that there is an unbalance. In such a case the current source, in this case I5, assumes a resistive character such that the currents into and out from the same current paths match. Similar occurrences occur for I3, I4 and I6. Also, In+ or In- may reach levels where I1 or I2 cannot function as current source. In this case those current sources assume a resistive character such that the current balance, but at those extremes the circuit will still operate.

Since there will always be currents through all the current legs in the load or current summation stage the common mode level at op and om and the differential can be controlled by the current levels and the transistor sizes as mentioned before to be lower than the Vcc and higher than ground.

It should be understood that above-described embodiments are being presented herein as examples and that many variations and alternatives thereof are possible. Accordingly, the present invention should be viewed broadly as being defined only as set forth in the hereinafter appended claims.

What is claimed is: